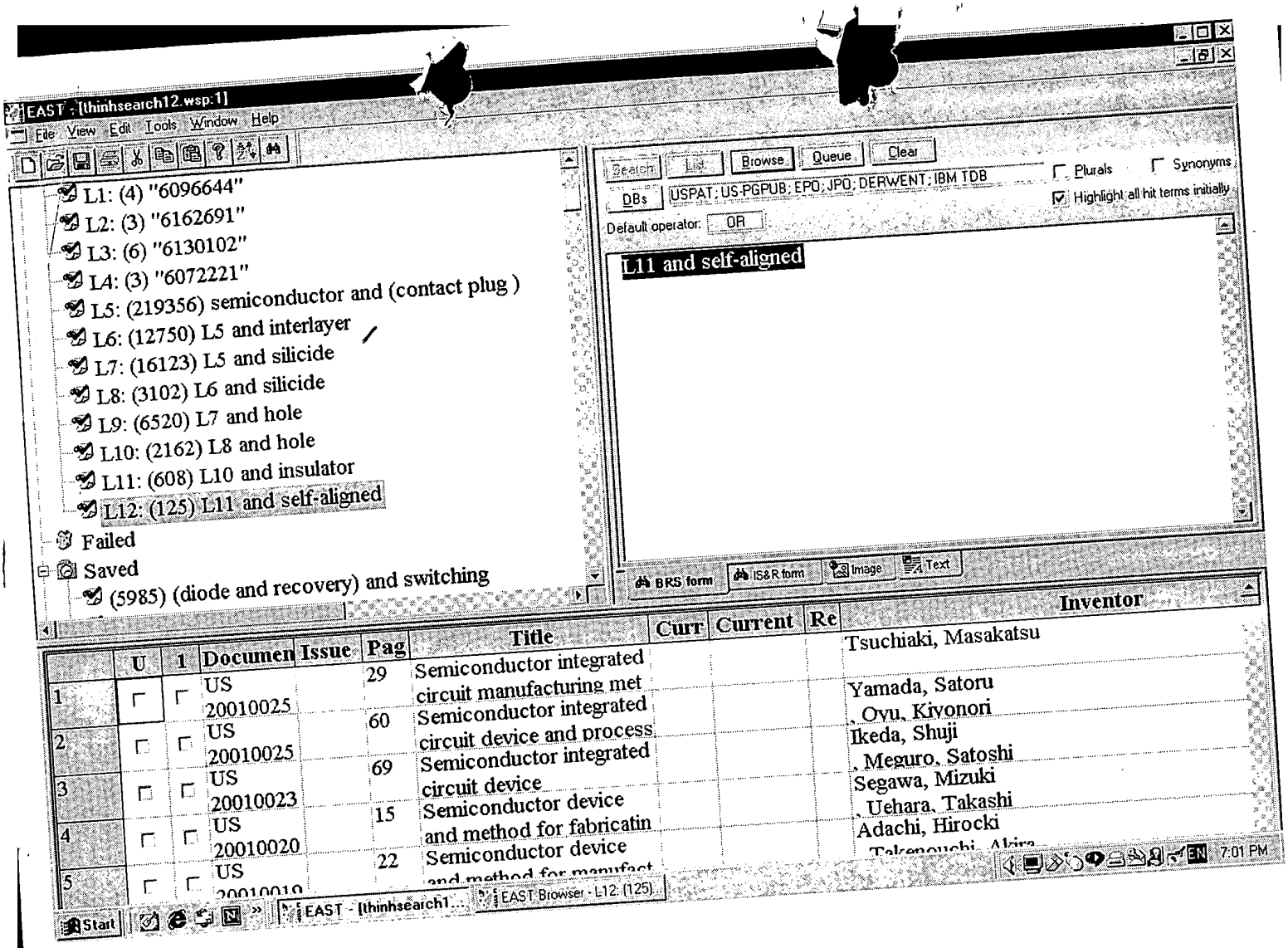
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L5: (219356) semiconductor and (contact plug)
L6: (12750) L5 and interlayer
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L8: (3102) L6 and silicide
L9: (6520) L7 and hole
L10: (2162) L8 and hole
L11: (608) L10 and insulator
L12: (125) L11 and self-aligned
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U 1 Documen Issue Pag Title Curr Current Re Inventor
1 US 20010025 29 Semiconductor integrated circuit manufacturing met Tsuchiaki, Masakatsu
2 US 20010025 60 Semiconductor integrated circuit device and process Yamada, Satoru , Oyu, Kiyonori
3 US 20010023 69 Semiconductor integrated circuit device Ikeda, Shuji , Meguro, Satoshi
4 US 20010020 15 Semiconductor device and method for fabricatin Segawa, Mizuki , Uehara, Takashi
5 US 22 Semiconductor device Adachi, Hirocki
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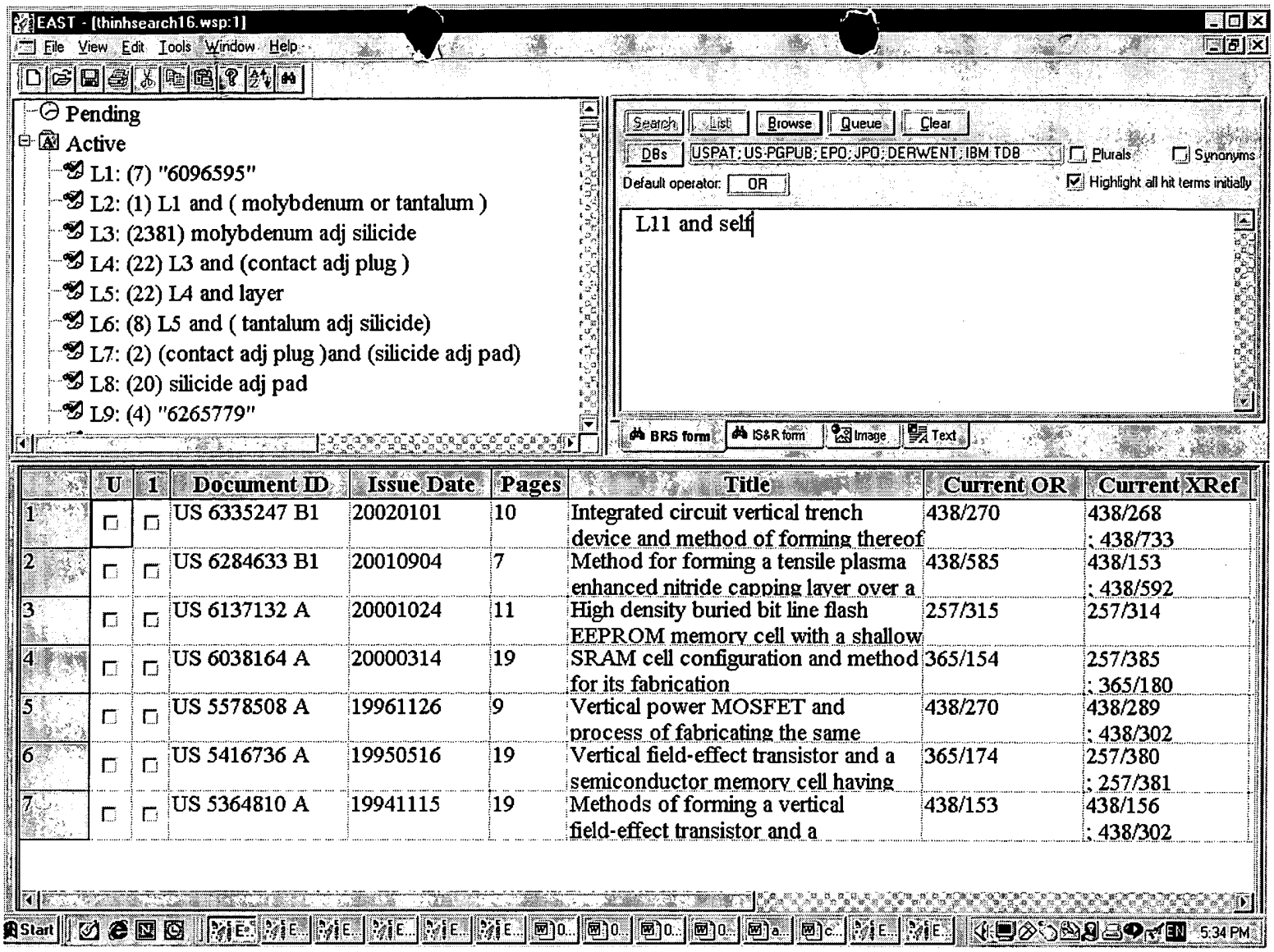
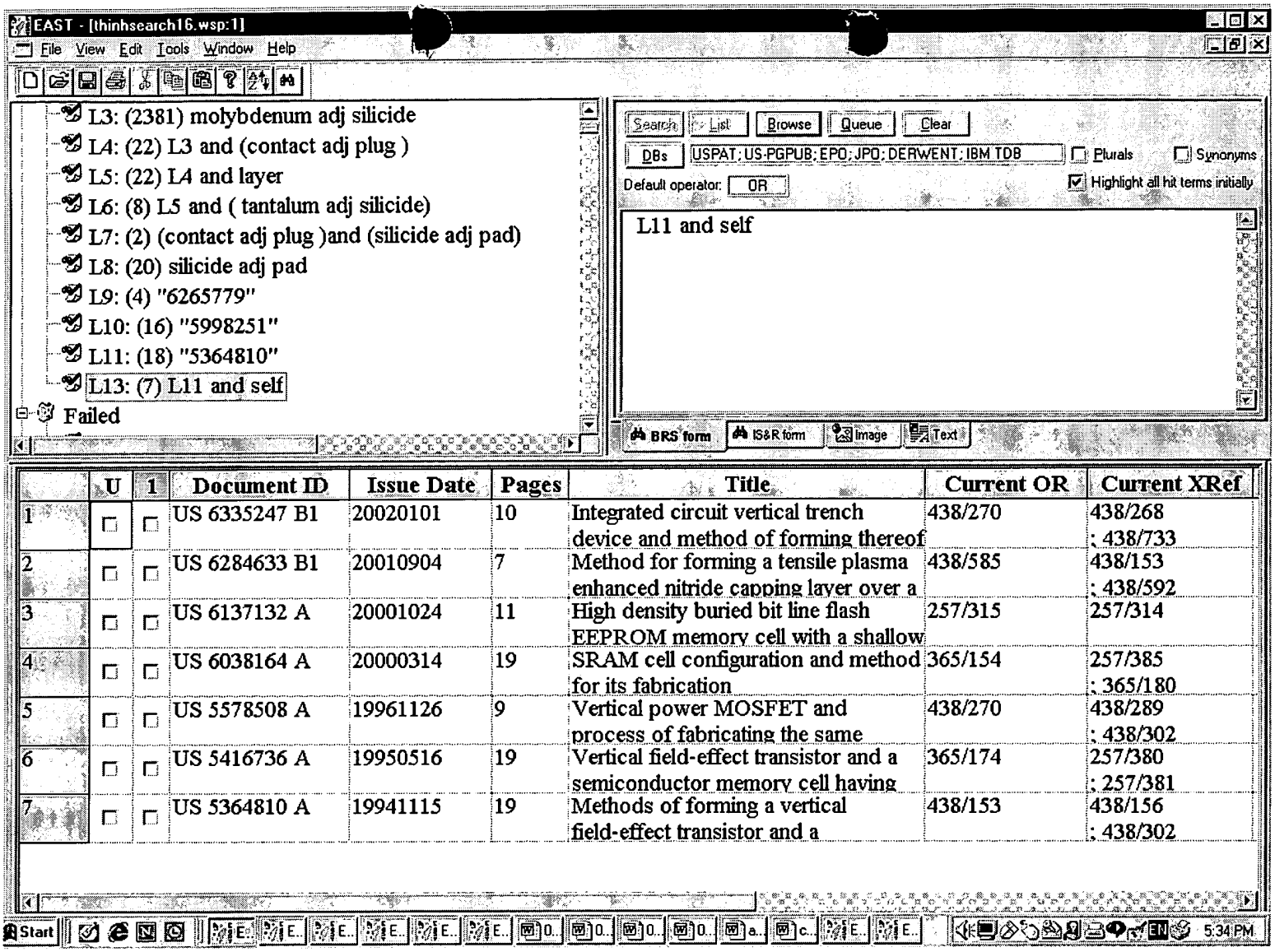


	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6335247 B1	20020101	10	Integrated circuit vertical trench device and method of forming thereof	438/270	438/268 ; 438/733
2	☐	☐	US 6284633 B1	20010904	7	Method for forming a tensile plasma enhanced nitride capping layer over a	438/585	438/153 ; 438/592
3	☐	☐	US 6137132 A	20001024	11	High density buried bit line flash EEPROM memory cell with a shallow	257/315	257/314
4	☐	☐	US 6038164 A	20000314	19	SRAM cell configuration and method for its fabrication	365/154	257/385 ; 365/180
5	☐	☐	US 5578508 A	19961126	9	Vertical power MOSFET and process of fabricating the same	438/270	438/289 ; 438/302
6	☐	☐	US 5416736 A	19950516	19	Vertical field-effect transistor and a semiconductor memory cell having	365/174	257/380 ; 257/381
7	☐	☐	US 5364810 A	19941115	19	Methods of forming a vertical field-effect transistor and a	438/153	438/156 ; 438/302



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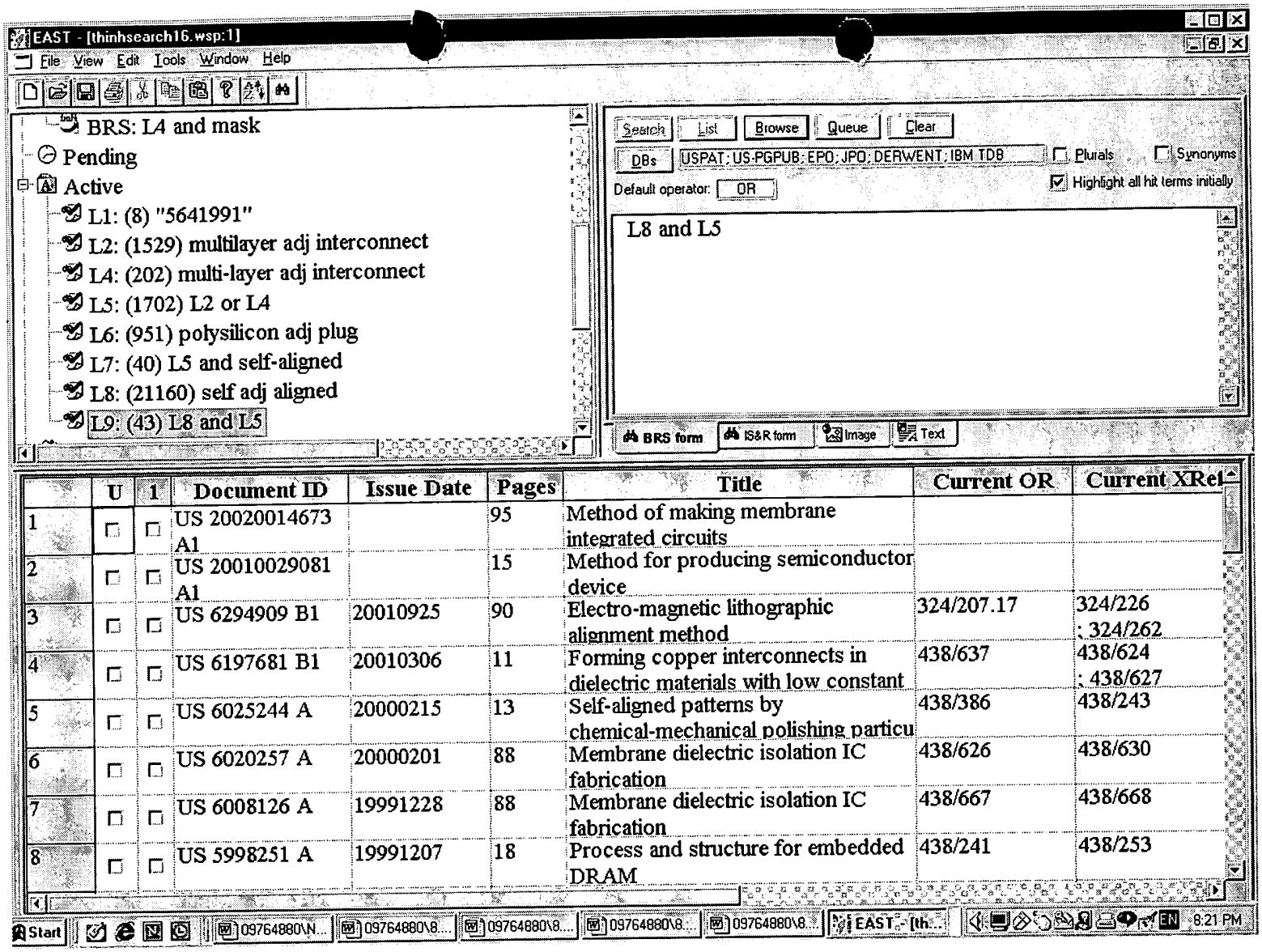

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1	☐	☐	US 20020014673 A1		95	Method of making membrane integrated circuits		
2	☐	☐	US 20010029081 A1		15	Method for producing semiconductor device		
3	☐	☐	US 6294909 B1	20010925	90	Electro-magnetic lithographic alignment method	324/207.17	324/226 ; 324/262
4	☐	☐	US 6197681 B1	20010306	11	Forming copper interconnects in dielectric materials with low constant	438/637	438/624 ; 438/627
5	☐	☐	US 6025244 A	20000215	13	Self-aligned patterns by chemical-mechanical polishing particu	438/386	438/243
6	☐	☐	US 6020257 A	20000201	88	Membrane dielectric isolation IC fabrication	438/626	438/630
7	☐	☐	US 6008126 A	19991228	88	Membrane dielectric isolation IC fabrication	438/667	438/668
8	☐	☐	US 5998251 A	19991207	18	Process and structure for embedded DRAM	438/241	438/253